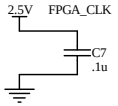
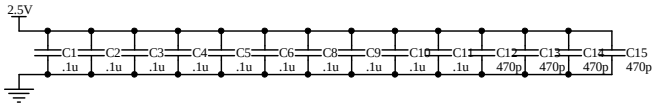
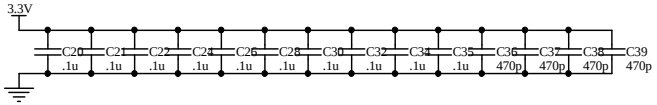
FPGA decoulping.

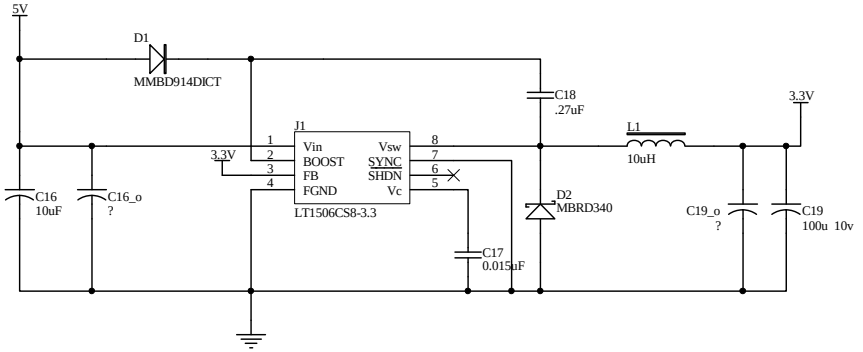
Los pines VCC_CLK y GND_CLK, no deben alimentarse de los planos de potencia. Se deben sacar lineas de alimentacion desde las salida de los conversores.

Los de 470p en paralelo deben de ser de alta frecuencia

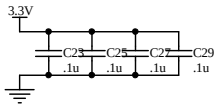




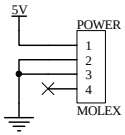


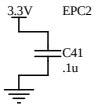


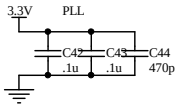
Memory decoulping.
4capacitors.
2 a cada lado

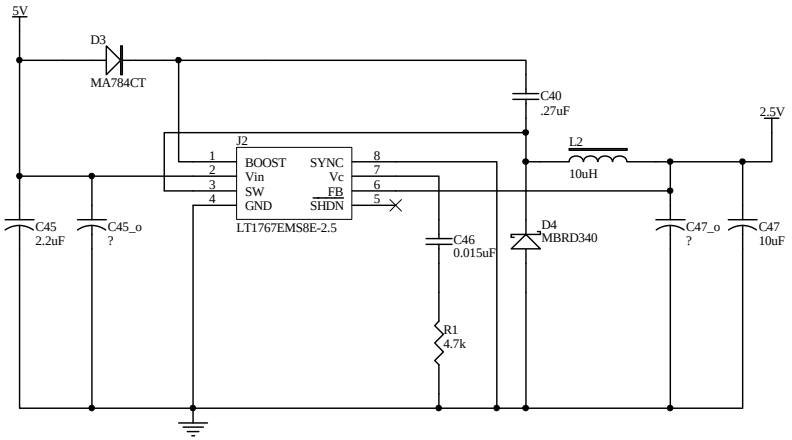


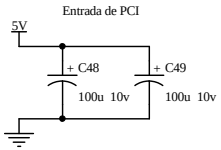
C?_o: Capacitores en paralelo para preveer la necesidad de bajar el ESR.

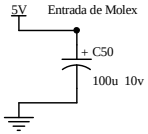












Title: IIE-PCI: Power conversion		
Size: B	Number:	Revision: Ver. 1.0
Date: 22-Dec-2003		Sheet of
File: H:\pci\proyecto\placa\version_1\pci\pci.ddb		Drawn By: